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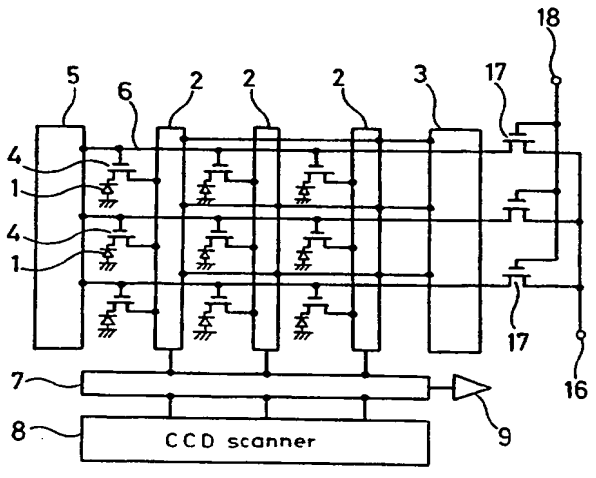
(54) A solid state imaging element.

(57) A solid state imaging element includes a plurality of photo detectors arranged in a two-dimensional array on a semiconductor substrate, two charge transfer circuits transferring signal charges in a vertical direction and a horizontal direction, respectively, a plurality of transfer gates controlling charge transfer from the photodetectors to one of the charge transfer circuits, a scanner controlling the switching of the transfer gates, a plurality of bus lines connecting the transfer gates with the scanner, and a bus line breakage checking means. This bus line breakage checking means includes a plurality of transistors connected with each of the bus lines in series, a test pad connected with the bus lines via the transistors and a voltage applying pad controlling the switching of the transistors. Therefore, the breakage of a bus line can be detected by a wafer test without actually operating the element, whereby time and cost required for the wafer test process and the assembly process can be reduced.

FIG. 1



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FIELD OF THE INVENTION

The present invention relates to a solid state imaging element which can be easily tested.

BACKGROUND OF THE INVENTION

Recently, accompanying with the advance of silicon LSI technology, solid state imaging elements in which a plurality of photodetectors are arranged in a two-dimensional array on a semiconductor substrate and these photodetectors are connected with a charge sweep device (hereinafter referred to as CSD) or a charge coupled device (hereinafter referred to as CCD) have been developed, and solid state imaging devices using such solid state imaging elements are put into practical use. Schottky-barrier diodes or photodiodes utilizing p-n junctions are usually employed for the photodetectors. Such solid state imaging elements are called "infrared imaging elements" or "visible light imaging elements" depending on the wavelength to be detected.

Figure 12 is a block diagram of an infrared CSD imaging device in which a plurality of infrared detectors are arranged on a silicon substrate and a scanning is carried out using CSD, disclosed in pages 42 to 48 of Defense Technology Journal, Vol.8, No.8, August 1987, published by Defense Technology Foundation. This device is constituted by a camera head 30, a signal processing part 31 and a monitor TV 33. In addition, this device employs a 512 X 512-element two-dimensional array type IRCSD (Infrared CSD) 32 as the imaging element. Since this IRCSD 32 performs electric circuit scanning, a mechanical scanner is dispensed with, resulting in a small sized and light-weight camera head 30. In addition, since the camera head 30 includes a Stirling cycle refrigerator 302 utilizing a closed cycle for cooling the infrared detectors down to 77 K, it is not necessary to provide a cooler.

An interline transfer CCD (hereinafter referred to as IL-CCD) is generally used for the charge transfer part of two-dimensional element. In this IL-CCD, as shown in figure 13, one potential well for vertical transfer is provided for one detector and signal charges are transferred in the vertical and horizontal directions by a so-called bucket brigading system. Although this IL-CCD has very low noise, there is a limitation in its charge transfer ability. More specifically, when the signal charge amount increases and signal charges from one pixel exceed the storage capacity of one bucket, the signal charges are mixed with those from another pixel. In order to avoid this, it is necessary to increase the dimension of the vertical CCD. However, when the dimension of vertical CCD is increased, the fill factor (the ratio of the photodetector area to the pixel size) decreases, resulting in a reduction in the sensitivity.

As another charge transfer system, there is a MOS system utilizing a MOS switch for reading out signals. The MOS system has an advantage over other systems in having a larger saturation charge amount. However, it has a disadvantage in that a large noise arises due to a large signal line capacitance and a fixed pattern noise arises due to variations in the characteristic of the MOS switch. Although a reduction in the pixel size is required to realize miniaturization and high resolution, such reduction in the pixel size induces a reduction in the signal charge amount obtained from one pixel. Thus, a large noise is a serious problem in the MOS system.

On the other hand, a CSD (Charge Sweep Device) used in the device of figure 12 is a new vertical charge transfer element, which realizes quite a large saturation charge amount with maintaining the noise level as high as that of the IL-CCD.

Description is given of the operation of the CSD with reference to figures 13 and 14, which are shown in pages 41 to 45 of a journal "Television Technology" of September 1985.

As shown in figure 13, the transfer gates of CSD are controlled separately from each other. Only a transfer gate is selected in a vertical row during a horizontal period. In figure 13, only the second transfer gate from the left is turned on and signal charges in the photodiode connected to the transfer gate are transferred to the CSD. Other photodiodes are accumulating signal charges at this time.

Above operation will be described in detail with reference to figure 14. In the CSD, the signal charges are transferred by the charge sweep-out operation, in which the potential wall pushes the signal charges to the horizontal CCD as shown in figures 14(b) to 14(d). A storage gate is provided between the horizontal CCD and the CSD, and the swept signal charges are stored in the storage gate as shown in figure 14(e). The sweep-out operation is completed in a horizontal period and the signal charges stored in the storage gate are transferred to the horizontal CCD during a horizontal blanking period as shown in figure 14(f) and then they are successively read out.

As described above, in the CSD, one vertical transfer element forms one potential well and the signal charges from one photodiode are output to the potential well. Therefore, sufficient signal charges can be obtained even when the channel width is reduced.

Figure 9 shows a structure of a conventional infrared solid-state imaging element including Schottky barrier diodes serving as photodetectors, CSDs serving as vertical charge transfer circuits and a CCD serving as a horizontal charge transfer circuit. In figure 9, reference numeral 1 designates infrared detectors such as PtSi/Si Schottky barrier diodes. Reference numeral 2 designates vertical CSDs for transferring signal charges and reference numeral 3 designates a CSD scanner for driving the vertical CSD 2. Reference numeral 4 designates transfer gates (TG) for controlling the charge transfer from the infrared detector 1 to the vertical CSD 2 and reference numeral 5 designates a TG scanner for driving the transfer gates 4. Reference numeral 6 designates bus lines connecting the transfer gates 4 with the TG scanner 5. Reference numeral 7 designates a horizontal CCD for transferring signal charges and reference numeral 8 designates a CCD scanner for driving the CCD 7. Reference numeral 9 designates an output amplifier.

Operation thereof will be described. Infared rays irradiated from the subject are incident on the photodetectors 1 arranged in a two-dimensional array and then converted into electricity in the photodetector 1. The signal charges thus generated are transferred to the vertical CSD 2 by opening the transfer gate 4. The switching of the transfer gate 4 is controlled by the TG scanner 5 connected to the transfer gate 4 by the bus line 6. When, the CSD scanner circuit 3 is driven, the signal charges in the vertical CSD 2 are transferred downward in the CSD 2 to reach the horizontal CCD 7. When the CCD scanner 8 is operated, the signal charges in the horizontal CCD 7 are transferred in the right direction in the CCD 7 to be output through the output amplifier 9. Then, signals from the photodetectors 1 arranged in a two-dimensional array are successively read out, whereby the intensity distribution of the infrared rays incident on the element is displayed on the monitor as an infrared image.

Figure 10 shows a structure of a conventional infrared solid state imaging element having Schottky barrier diodes as photodetectors in which the signal charges are read out by MOS system. In figure 10, reference numeral 1 designates infrared detectors such as PtSi/Si Schottky barrier diodes. Reference numeral 10 designates vertical MOS transistors for reading out signal charges and reference numeral 11 designates a vertical scanner for controlling the switching of the vertical MOS transistors 10. Reference numeral 12 designates bus lines connecting the vertical MOS transistors 10 with the vertical scanner 11. Reference numeral 13 designates a horizontal MOS transistor for reading out signal charges and reference numeral 14 designates a horizontal scanner for controlling the switching of the horizontal MOS transistors 13. Reference numeral 15 designates bus lines connecting the horizontal MOS transistors 13 with the horizontal scanner 14. Reference numeral 9 designates an output amplifier.

Operation thereof will be described. Infared rays irradiated from the subject are incident on the photodetectors 1 arranged in a two-dimensional array and then converted into electricity in the photodetectors 1 similarly as in figure 9. The signal charges thus generated are read out by MOS system. More specifically, the signal charges from the photodetector 1 provided on a point where a bus line 12 in transverse direction selected by the vertical scanner 11 intersects a bus line 15 in longitudinal direction selected by the horizontal scanner 14 are output through the output amplifier 9. The signal charges from the photodetectors 1 arranged in a two-dimensional array are successively read out and then the intensity distribution of the infrared rays incident to the element are displayed on the monitor as an infrared image.

Figure 11 shows a structure of a conventional infrared solid-state imaging element having Schottky barrier diodes as photodetectors and CCDs as vertical and horizontal charge transfer circuits. In figure 11, reference numeral 1 designates infrared detectors such as PtSi/Si Schottky barrier diodes. Reference numeral 13 designates vertical CCDs for transferring signal charges and reference numeral 14 designates a CCD scanner for driving the CCDs. Reference numeral 4 designates transfer gates (TG) for controlling the charge transfer from the infrared detectors 1 to the vertical CCD 13. Reference numeral 15 designates an input pin for inputting a clock signal for driving the transfer gates 4. Reference numeral 6 designates bus lines connecting the input pin 15 with the transfer gates 4. Reference numeral 7 designates a horizontal CCD for transferring signal charges and reference numeral 8 designates a CCD scanner for driving the horizontal CCD 7. Reference numeral 9 designates an output amplifier.

In this infrared imaging element, unlike the infrared imaging element shown in figure 9, CCD is used for the charge transfer in vertical direction. The operation thereof is fundamentally the same as that of the element shown in figure 9 except for that the switching of the transfer gate 4 is controlled by the clock signal applied to the input pin 15 and the vertical CCDs 13 are controlled by the CCD scanner 14.

The infrared solid-state imaging elements shown in figures 9, 10 and 11 are formed by a silicon LSI process. During the process, breakage of Al wirings for the bus lines 6, 12 and 15 may occur.

When the bus line 6 is broken in the infrared solid state elements shown in figures 9 and 11, the transfer gate 4 on the right of the broken bus line in the figure cannot be opened and the signal charges from the photodetectors 1 cannot be read out. As a result, in the solid-state imaging element including such a broken bus line, an image defect A having continuous insensitive portions in the transverse direction as shown in figure 15 appears on the output image.

When the bus lines 12 and 15 are broken in the infrared solid-state imaging element shown in figure 10, an image defect A or B having continuous insensitive portions in the transverse direction or the longitudinal direction appears on the output image. In addition, when the diode is faulty or the contact part of the transfer gate is opened, a black spot defect C as shown in figure 15 appears.

As a method for detecting such defects, there is a method of detecting the output image by driving an assembled element. This makes even elements including defects pass through a wafer test process or an assembly process, resulting in that much time and high cost are unfavorably required for each process.

As another method for detecting these defects, there is a method of driving the element in a wafer test. In a case of an infrared imaging element using Schottky barrier diodes, it is necessary to cool the element down to approximately 77 K to operate the detector. However, it is technically difficult to perform a wafer test at such a low temperature.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a solid-state infrared imaging element which can detect a transverse black line defect or a longitudinal black line defect, i.e., a breakage of a bus line by a wafer test without actually operating the element.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the spirit and the scope of the invention will become apparent to those skilled in the art from this detailed description.

In accordance with the present invention, a solid state imaging element includes a checking means for detecting a breakage of a bus line.

Therefore, the breakage of a bus line can be detected at a room temperature without actually operating the element.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of an infrared imaging element which reads out signal charges by CSD system in accordance with a first embodiment of the present invention;

Figure 2 is a schematic diagram showing a fundamental structure of a bus line breakage checking circuit in accordance with the first embodiment of the present invention;

Figure 3 is a schematic diagram of an infrared imaging element which reads out signal charges by MOS system in accordance with a second embodiment of the present invention;

Figure 4 is a schematic diagram of an infrared imaging element which reads out signal charges by CSD system in accordance with a third embodiment of the present invention;

Figures 5 and 6 are schematic diagrams showing fundamental structures of bus line breakage checking circuits in accordance with the third embodiment of the present invention;

Figure 7 is a schematic diagram of an infrared imaging element which reads out signal charges by CCD system in accordance with a fourth embodiment of the present invention;

Figure 8 is a schematic diagram of an infrared imaging element which reads out signal charges by MOS system in accordance with a fifth embodiment of the present invention;

Figure 9 is a schematic diagram of an infrared imaging element of CSD system in accordance with the prior art;

Figure 10 is a schematic diagram of an infrared imaging element of MOS system in accordance with the prior art;

Figure 11 is a schematic diagram of an infrared imaging element of CCD system in accordance with the prior art;

Figure 12 is a block diagram of an infrared imaging device;

Figures 13 and 14 are diagrams showing a structure and a charge sweep-out operation of a basic CSD system; and

Figure 15 is a diagram showing image defects appearing on an output image.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail with reference to the drawings.

Figure 1 is a schematic diagram showing a structure of an infrared imaging element which reads out signal charges by CSD system in accordance with a first embodiment of the present invention. Figure 2 is a schematic diagram showing a

fundamental structure of a bus line breakage checking circuit in accordance with the present invention.

In figure 1, reference numerals 1 to 9 designate the same elements as those shown in figure 9. Reference numeral 16 designates a pad for detecting breakage of a wire in transverse direction from the outside. Each bus line 6 is connected with the pad 16 by the transistors 17. Reference numeral 18 designates a gate voltage applying pad for controlling the switching of the transistors 17. The transistors 17 and the pads 16 and 18 constitute a circuit for detecting breakage of a bus line.

When this infrared imaging element is operated, the pad 18 is short-circuited with the substrate to turn off the transistors 17. At this time, the breakage checking circuit is electrically separated from the bus line 6 and then an infrared image is obtained by the same operation as in the conventional example of figure 9.

When the breakage of a bus line is detected, a wafer test will be carried out in accordance with the following process. First, a gate voltage is applied to the pad 18 to turn on the transistors 17, thereby to connect the pad 16 with the bus lines 6. In this state, the TG scanner 5 is operated and the pulse voltage applied to each bus line 6 by the scanner circuit 5 is monitored from the pad 16. The TG scanner 5 applies a high level to a selected bus line and a low level to other non-selected bus lines while the element operates. In a state where the breakage checking circuit is connected, however, a current flows from the selected bus line to the non-selected bus lines via this breakage checking circuit, so that a normal scanning is not carried out. Therefore, in this wafer test, the non-selected bus lines are opened, not applied with a low level to these bus lines. The pulses monitored from the pad 16 are pulses sent from the scanner 5 when there is no breakage of the bus line, while lack of pulse of the same number as the broken bus lines occur when there is breakage of the bus line. Thus, the breakage of the bus line is detected.

Figure 3 is a schematic diagram showing a structure of an infrared imaging element which reads out signal charges by MOS system in accordance with a second embodiment of the present invention. In figure 3, reference numerals 1 and 9 to 15 designate the same elements as those shown in figure 10. Reference numeral 19 designates a pad for detecting breakage of bus lines 12 in transverse direction from outside. Each bus line in transverse direction is connected with the pad 19 by the transistors 20. Reference numeral 21 designates a gate voltage applying pad for controlling the switching of the transistors 20. Reference numeral 22 designates a pad for detecting breakage of bus lines 15 in longitudinal direction from the outside. Each bus line in longitudinal direction is connected with the pad 22 by the transistors 23. Reference numeral 24 designates a gate voltage applying pad for controlling the switching of the transistors 23. The transistors 20 and the pads 19 and 21 constitute a bus line breakage checking circuit in transverse direction and the transistors 23 and the pads 22 and 24 constitute a bus line breakage checking circuit in longitudinal direction.

In this second embodiment, the two breakage checking circuits 19 to 21 and 22 to 24 have the same structure as that of the breakage checking circuit shown in figure 2. Accordingly, a wafer test can be carried out in accordance with the same process as described in the first embodiment of the present invention. More specifically, when the element is operated, the pads 21 and 24 are short-circuited with the substrate to turn off the transistors 20 and 23. At this time, the two breakage checking circuits are electrically isolated from the bus lines 12 and 15 and an infrared image can be obtained by the same operation as in the convention example of figure 10.

When, the breakage of the bus line in transverse direction is detected, the pulse from the vertical scanner 11 is monitored by the pad 19 by the same way as in the first embodiment. When the breakage of the bus line in longitudinal direction is detected, the pulse from the horizontal scanner 14 is monitored by the pad 22.

While the breakage checking circuits of above-described first and second embodiments are appropriate for detecting which bus line is broken, third to fifth embodiments which will be described hereinafter provide breakage checking circuits for only detecting the existence of a broken bus line.

Figure 4 is a schematic diagram showing a structure of an infrared imaging element which reads out signal charge by CSD system in accordance with a third embodiment of the present invention. Figures 5 and 6 are schematic diagrams showing fundamental structures of the breakage checking circuits.

In figure 4, reference numerals 1 to 9 designate the same elements as those shown in figure 9. Reference numeral 10 designates two pads for detecting breakage of a bus line from the outside. All bus lines are connected with the two pads 10 in series by the transistors 11. Reference numeral 12 designates a gate voltage applying pad for controlling the switching of the transistors 11. The transistors 11 and the pads 10 and 12 constitute a breakage checking circuit.

Figure 5 shows the breakage checking circuit of the infrared imaging element of figure 4. In these figures, reference numerals 10 to 12 designate the

same elements as those shown in figure 4 and reference numeral 6 designates n pieces of bus lines.

In the infrared imaging element of figure 4, when the element is operated, the pad 12 is short circuited with the substrate to turn off the transistor 11. At this time, the breakage checking circuit is electrically separated from the bus line 6 and then an infrared image is obtained by the same operation as in the conventional example of figure 9.

When the breakage of the bus line is detected, a wafer test is carried out in accordance with the following process. First, the CSD scanner 3 is electrically separated from the TG scanner 5. In this state, the circuit shown in figure 4 is electrically equivalent to the circuit shown in figure 5. In figure 5, a gate voltage is applied to the pad 12 to turn on the transistors 11, thereby to connect the two pads 10 with the n pieces of bus lines in series. In this state, it is checked whether current flows between the two pads 10 or not, whereby the breakage of bus line can be detected.

In figure 5, the breakage checking circuit is constituted by n pieces of bus lines 6 and (n + 1) pieces of transistors 11. This breakage checking circuit can be constituted by n pieces of bus lines 6 and (n-1) pieces of transistors 11 as shown in figure 6.

Figure 7 is a schematic diagram showing a structure of an infrared imaging element which reads out signal charges by CCD system in accordance with a fourth embodiment of the present invention. In figure 7, reference numerals 1, 4, 6 to 9, and 13 to 15 designate the same elements as those shown in figure 11. Reference numerals 10 to 12 designate the breakage checking circuit shown in figure 5. Preference numeral 16 designates transistors connecting each bus line 6 in transverse direction with the input pin 15, and reference numeral 17 designates a gate voltage applying pad for controlling the switching of the transistors 16.

When this infrared imaging element operates, the pad 12 is short circuited with the substrate to turn off the transistors 11, whereby the breakage checking circuit is electrically separated from the bus lines 6. Then, a gate voltage is applied to the pad 17 to turn on the transistors 16, whereby the clock input pin 15 is connected with each bus line 6 in parallel. In this state, the circuit shown in figure 7 is electrically equivalent to the circuit shown in figure 11 and an infrared image can be obtained by the same operation as in the conventional example of figure 11.

When the breakage of the bus line is detected, the pad 17 is short circuited with the substrate to turn off the transistors 16, whereby the bus lines connected in parallel are separated from each other. Then, the CCD scanner 14 is electrically separated from the vertical CCD. In this state, the circuit shown in figure 7 is electrically equivalent to the circuit shown in figure 5 and the breakage of bus line can be detected by the same way as in the third embodiment.

Figure 8 is a schematic diagram showing a structure of an infrared imaging element which reads out signal charges by MOS system in accordance with a fifth embodiment of the present invention. In figure 8, reference numerals 1, 6a, 6b, 9, 18 to 21 designate the same elements as those shown in figure 10. Reference numerals 10a to 12a and 10b to 12b designate the breakage checking circuit shown in figure 5, respectively.

The infrared imaging element of MOS system shown in figure 8 has the bus lines 6a in the longitudinal direction and the bus lines 6b in the transverse direction. Therefore, this infrared imaging element has a structure in which the breakage checking circuit shown in figure 5 is provided in the transverse direction and the longitudinal direction of the infrared imaging element shown in figure 10. When the element is operated, the breakage checking circuit 10a to 12a and the breakage checking circuit 10b to 12b are electrically separated from each other, and then an infared image can be obtained by the same operation as in the conventional example of figure 10. In addition, when the vertical scanner 19 and the horizontal scanner 21 are electrically separated from each other, the circuit shown in figure 8 is equivalent to the two breakage checking circuits shown in figure 5, so that the breakage of the bus line can be detected in the both directions by the same way as in the above third embodiment.

In the above-described first to fifth embodiments, infrared imaging elements using Schottky barrier diodes for the photodetectors are described. However, the present invention can be applied to infrared imaging elements or visible imaging elements using other photodetectors.

In addition, as the signal reading out systems, CSD system, CCD system, and MOS system are used in the above embodiments. However, the breakage of the bus line can be detected using the breakage checking circuit of figure 5 or 6 also in a solid state imaging element having another reading out system, as far as it has bus lines in transverse direction or longitudinal direction.

In the above described first to fifth embodiments, since a breakage checking circuit for detecting breakage of a bus line is provided on an infrared imaging element, it is possible to detect which bus line is broken in the first and second embodiments, and it is possible to detect the existence of a broken bus line in the third and fourth embodiments. Therefore, time and cost required

for the wafer test process and the assembly process can be reduced. In addition, since an identification of the broken bus line can be performed by the wafer test, the breakage checking circuit of the present invention is also effective for a failure analysis.

Claims

1. A solid state imaging element comprising:

a plurality of photo detectors arranged in a two-dimensional array on a semiconductor substrate;

two charge transfer circuits transferring signal charges in a vertical direction and a horizontal direction, respectively;

a plurality of transfer gates controlling charge transfer from said photodetectors to one of said charge transfer circuits;

a scanner controlling the switching of said transfer gates;

a plurality of bus lines connecting said transfer gates with said scanner; and

a bus line breakage checking means including a plurality of transistors connected with each of said bus lines in series, a test pad connected with said bus lines via said transistors, and a voltage applying pad controlling the switching of said transistors.

2. A solid state imaging element comprising:

a plurality of photodetectors arranged in a two-dimensional array on a semiconductor substrate;

a plurality of MOS transistors reading out signal charges and connected with said photodetectors; two scanner circuits in a vertical direction and a horizontal direction, each controlling the reading out of signal charges;

a plurality of bus lines in a vertical direction and a horizontal direction for connecting said MOS transistors with said scanner circuits; and

at least one set of a bus line breakage checking means in a vertical direction and a bus line breakage checking means in a horizontal direction, each including a plurality of transistors connected with said bus lines in series, a test pad connected with said transistors via said bus lines, and a voltage applying pad controlling the switching of said transistors.

3. A solid state imaging element comprising:

a plurality of photodetectors arranged in a two-dimensional array on a semiconductor substrate;

two circuits for reading out signal charge in a vertical direction and a horizontal direction, respectively;

a plurality of gate transistors controlling charge transfer from said photodetectors to said signal charge reading out circuits;

a scanner controlling the switching of said gate transistors;

a plurality of bus lines connecting said gate transistors with said scanner;

at least one bus line breakage checking means including a plurality of transistors connecting said bus lines in a transverse direction and a longitudinal direction respectively in series, two test pads provided at both ends of said bus line and connected through said transistors, and a gate voltage applying pad for controlling the switching of said transistors.

4. A solid state imaging element of claim 3 wherein the switching of said gate transistors are controlled by an external clock input pin which is connected with said gate transistors via said bus lines.

5. A solid state imaging element of claim 1 wherein a gate voltage is applied to said voltage applying pad to turn on said transistors, said test pad is connected with said bus lines to operate said scanner, a voltage is applied to a selected bus line, non-selected bus lines are opened to be electrically isolated, and pulse voltage applied to said bus lines by said scanner is monitored from said test pad.

6. A solid state imaging element of claim 2 wherein when the breakage of said transverse direction bus line is detected, a gate voltage is applied to said voltage applying pad to turn on said transistors, said test pad is connected with said bus lines to operate said scanner, a voltage is applied to a selected bus line, non-selected bus lines are opened to be electrically isolated, and a pulse from said vertical scanner is monitored by said test pad in transverse direction; and

when the breakage of said bus line in longitudinal direction is detected, a pulse from said horizontal scanner is monitored from said test pad in longitudinal direction.

7. A solid state imaging element of claim 3 wherein when the breakage of bus line in a transverse or longitudinal direction is detected, said voltage applying pad is short circuited with said substrate, said transistors are turned off to open the parallel connection of said bus lines, CCD scanner is electrically isolated, and said two test pads are serially connected with n pieces of bus lines to detect whether current flows between said two pads or not.

8. A solid state imaging element of claim 1 wherein Schottky barrier diodes are used for said photodetectors.

9. A solid state imaging element of claim 2 wherein Schottky barrier diodes are used for said photodetectors.

9. A solid state imaging element of claim 3 wherein Schottky barrier diodes are used for said photodetectors.

10. A solid state imaging element of claim 1 wherein CCD is used for said horizontal signal charge reading circuit and said vertical signal charge reading circuit.

11. A solid state imaging element of claim 2 wherein CCD is used for said horizontal signal charge reading out circuit and said vertical signal charge reading circuit.

12. A solid state imaging element of claim 3 wherein CCD is used for said horizontal signal charge reading circuit and said vertical signal charge reading circuit.

13. A solid state imaging element of claim 1 wherein CCD is used for said horizontal signal charge reading circuit and CSD is used for said vertical direction signal charge reading circuit.

14. A solid state imaging element of claim 2 wherein CCD is used for said horizontal signal charge reading circuit and CSD is used for said vertical direction signal charge reading circuit.

15. A solid state imaging element of claim 3 wherein CCD is used for said horizontal signal charge reading circuit and CSD is used for said vertical direction signal charge reading circuit.

FIG. 1

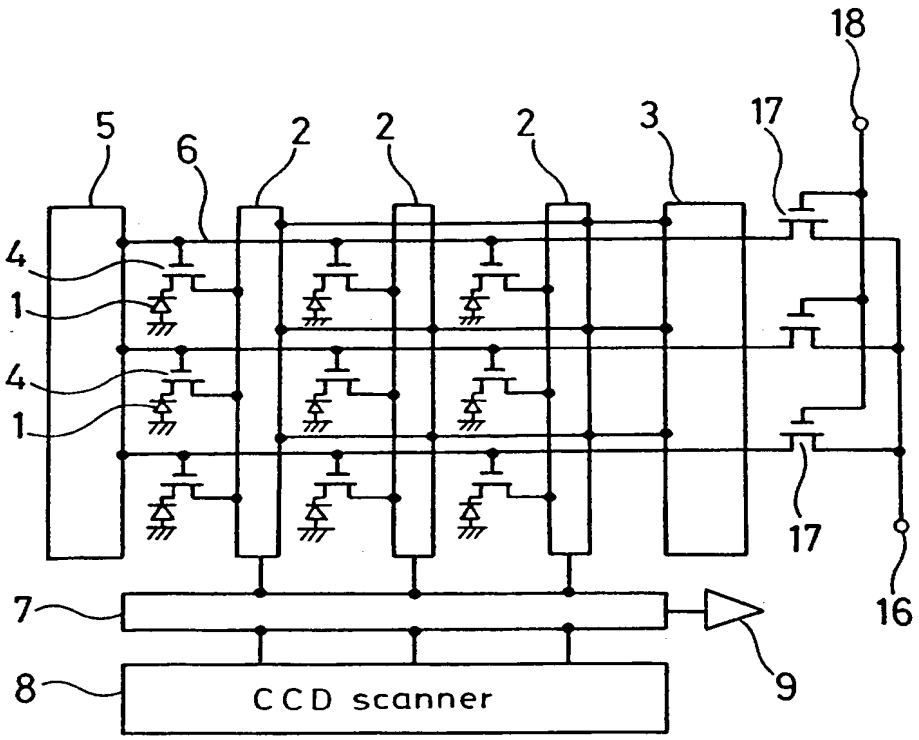


FIG. 2

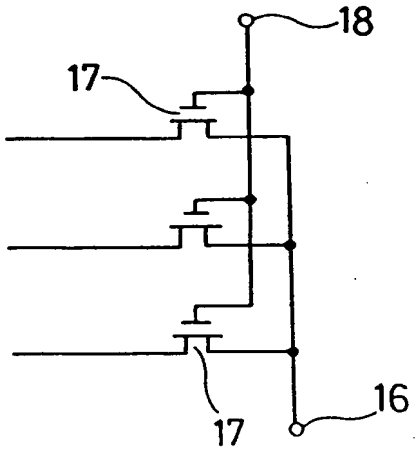


FIG. 3

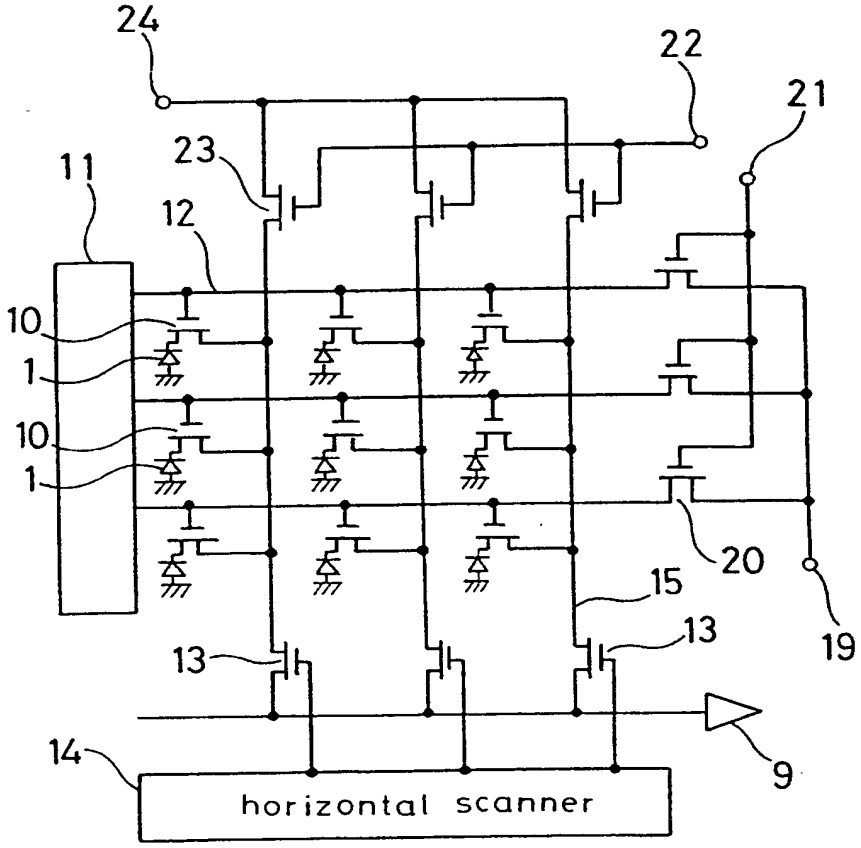


FIG. 4

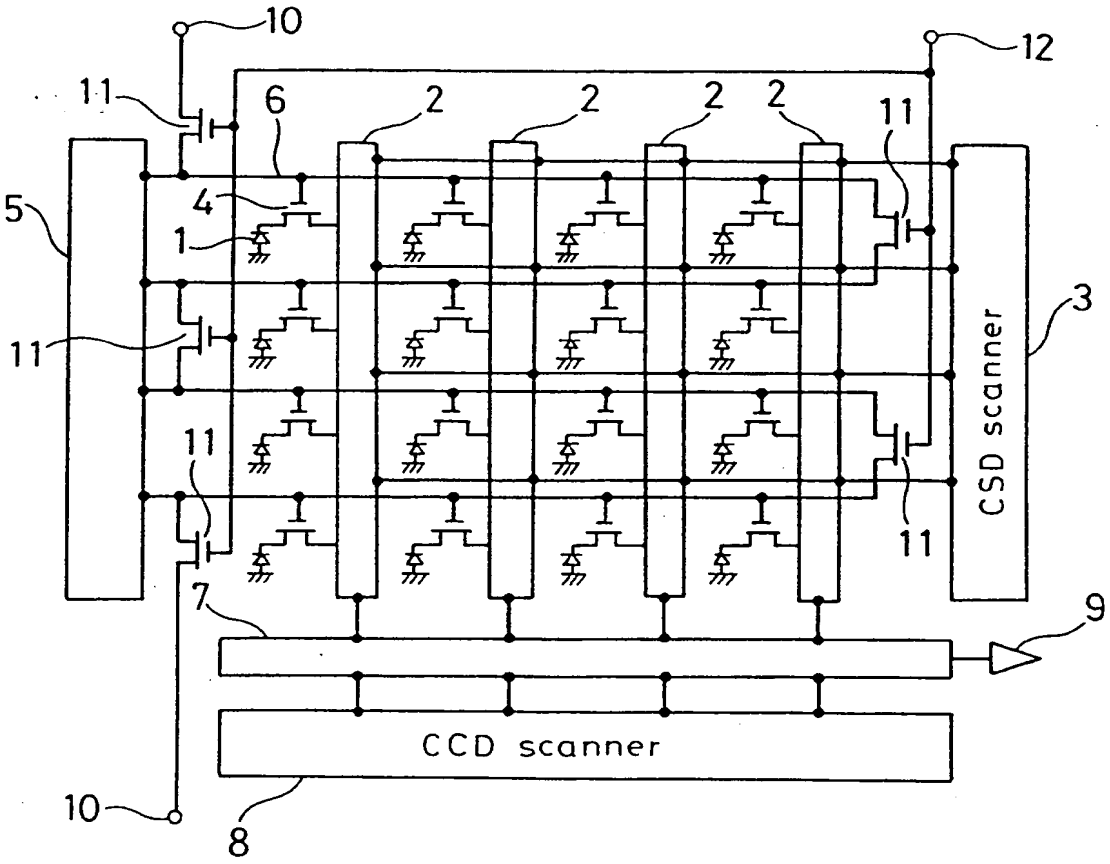


FIG. 5

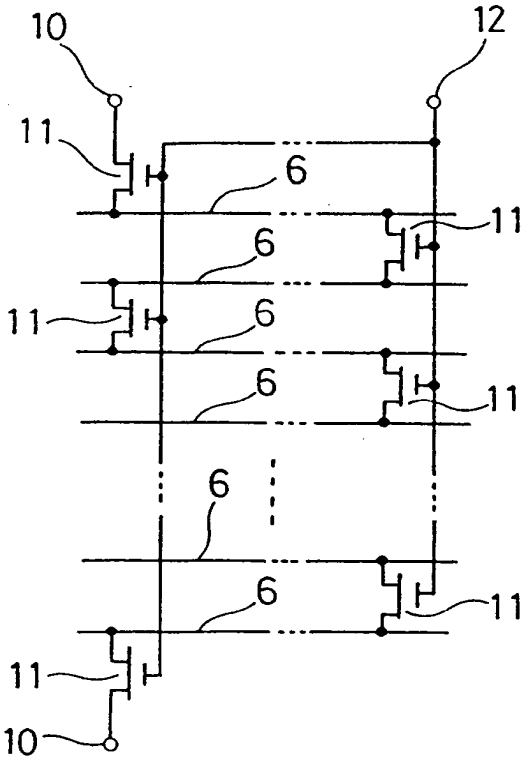


FIG. 6

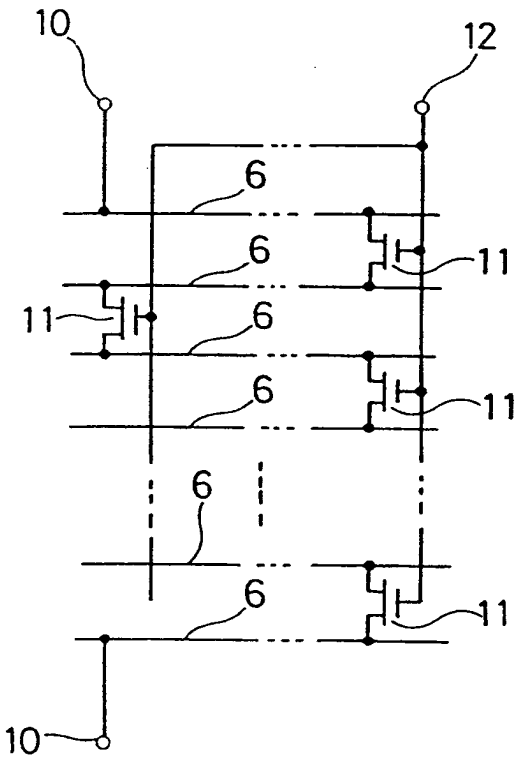


FIG. 7

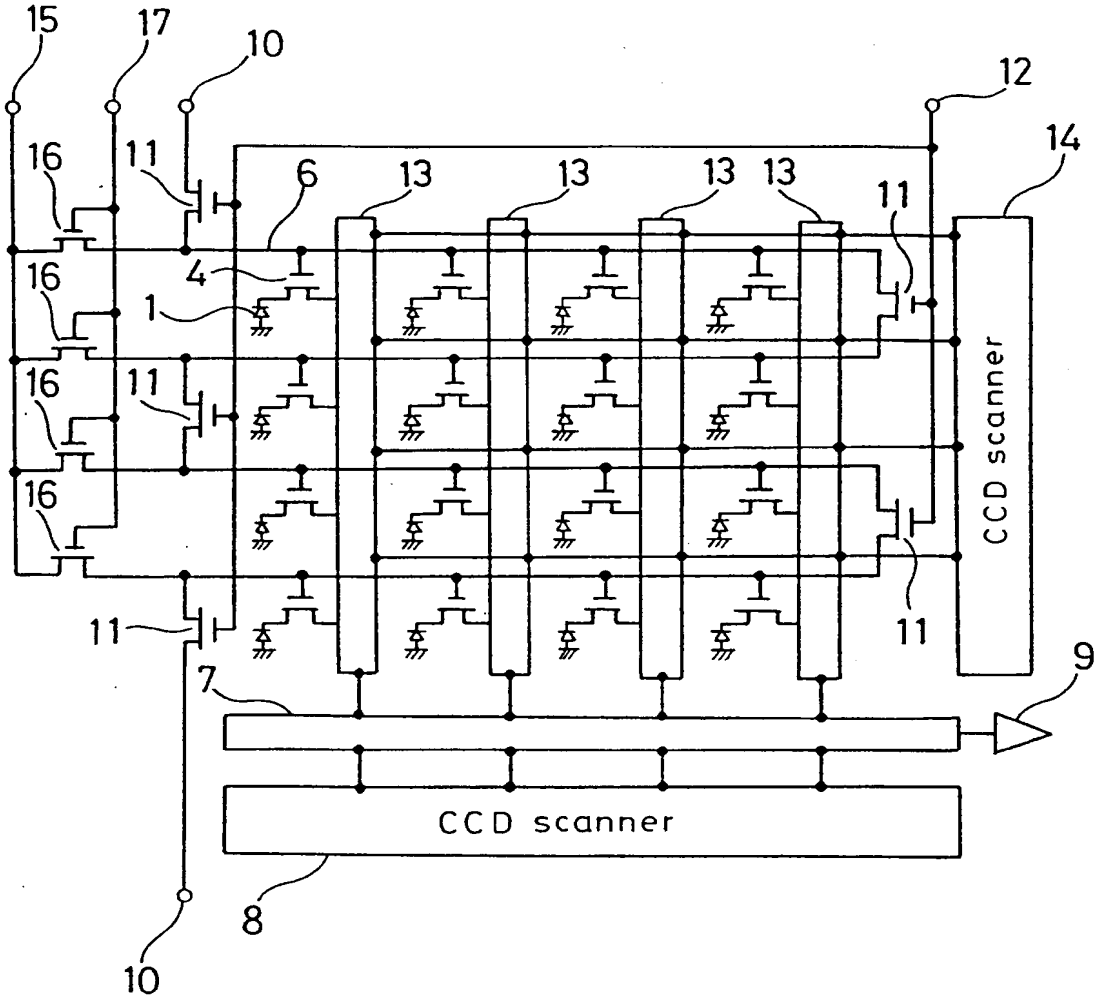


FIG. 8

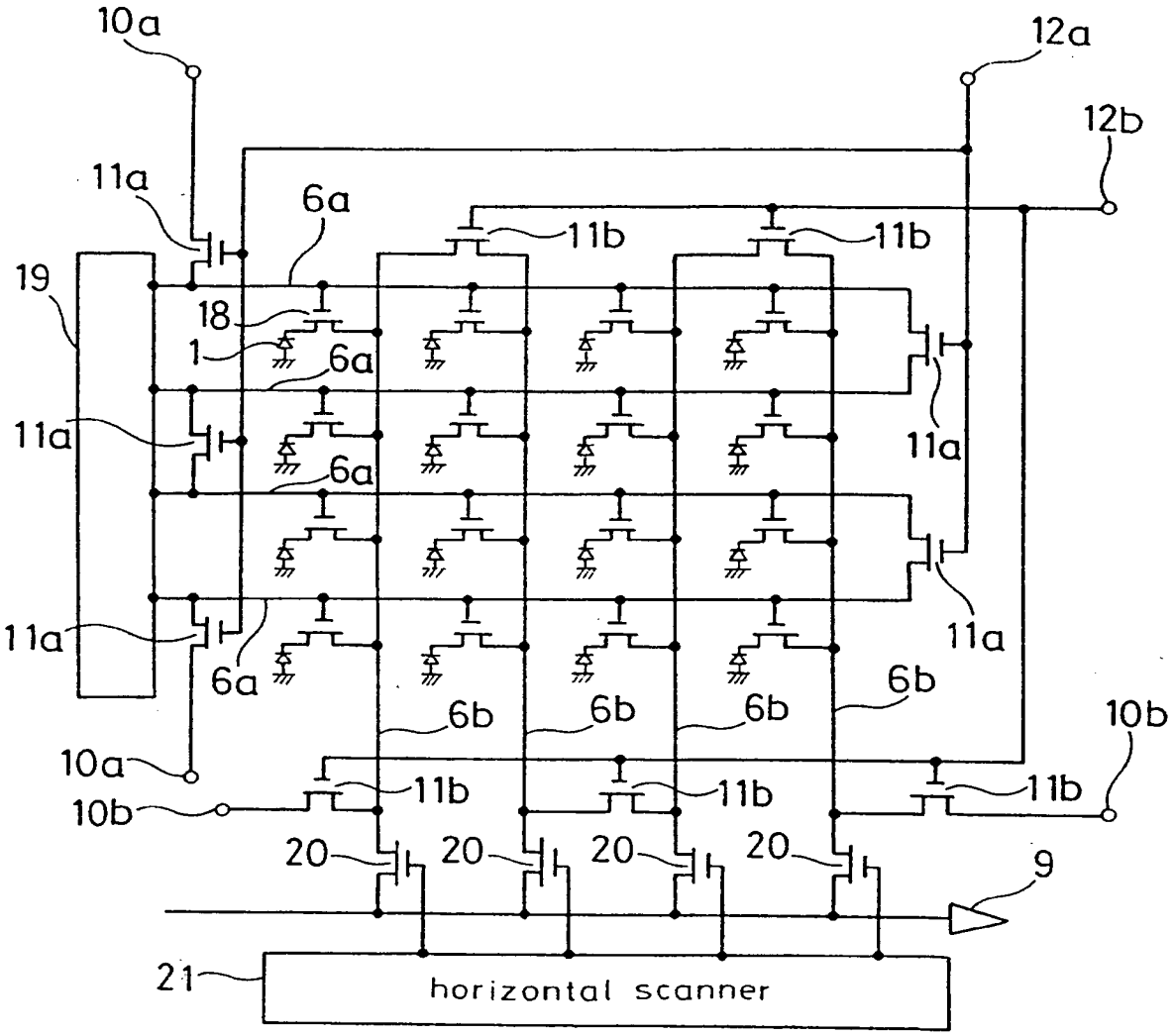


FIG. 9 (PRIOR ART)

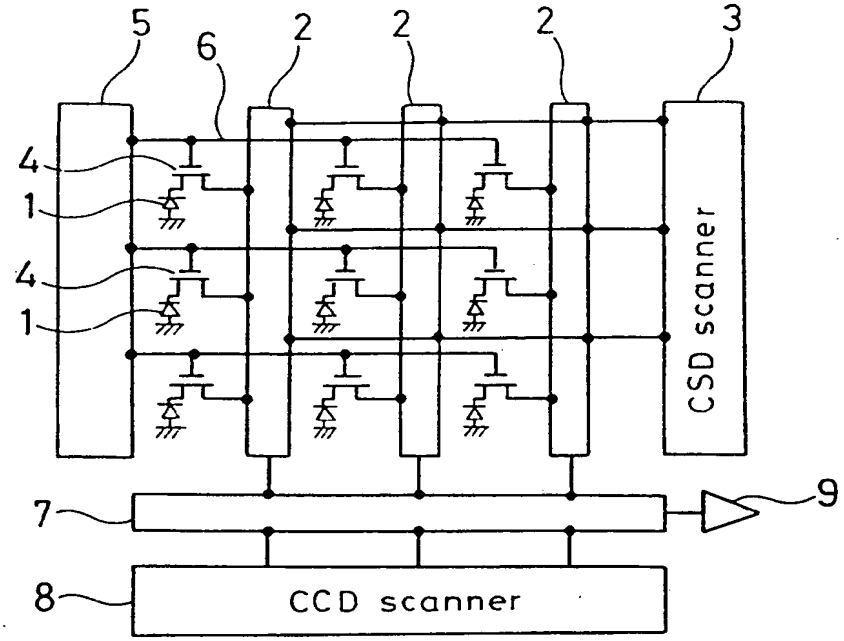


FIG. 10 (PRIOR ART)

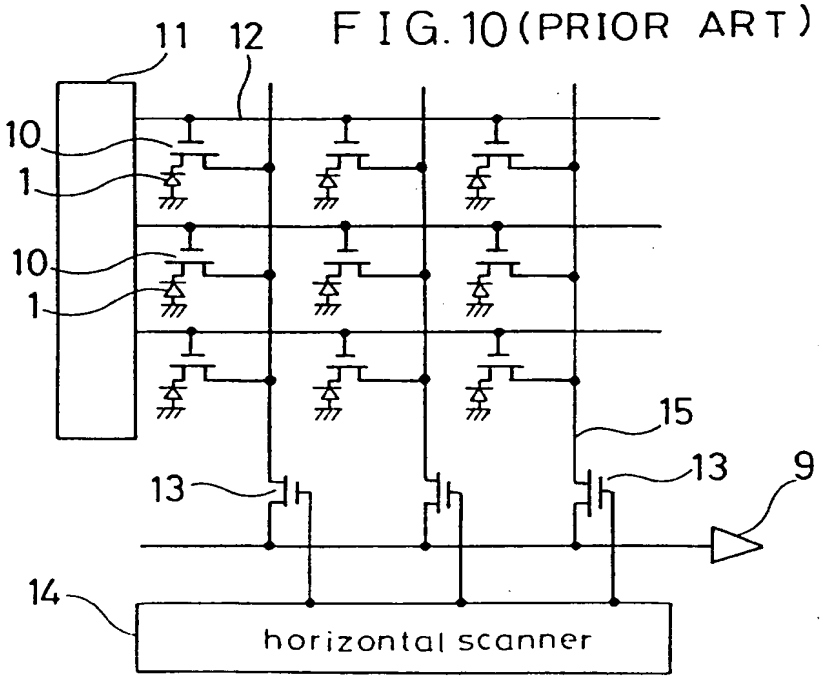


FIG. 11 (PRIOR ART)

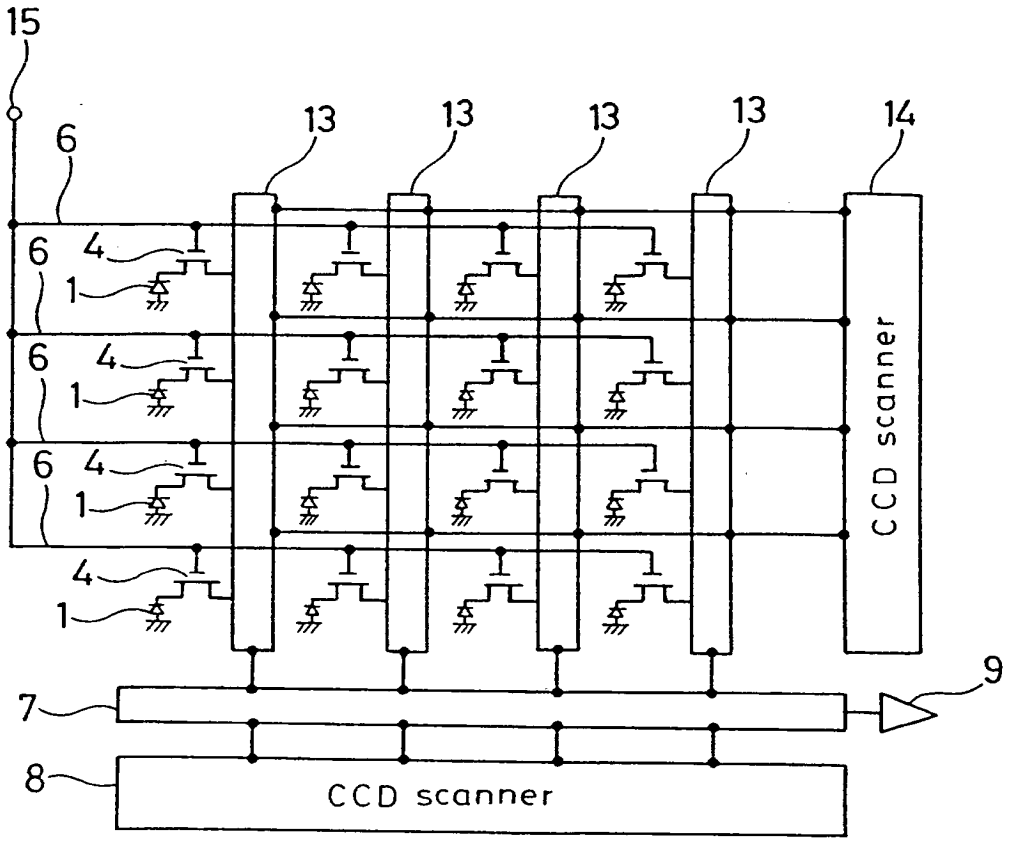


FIG. 12 (PRIOR ART)

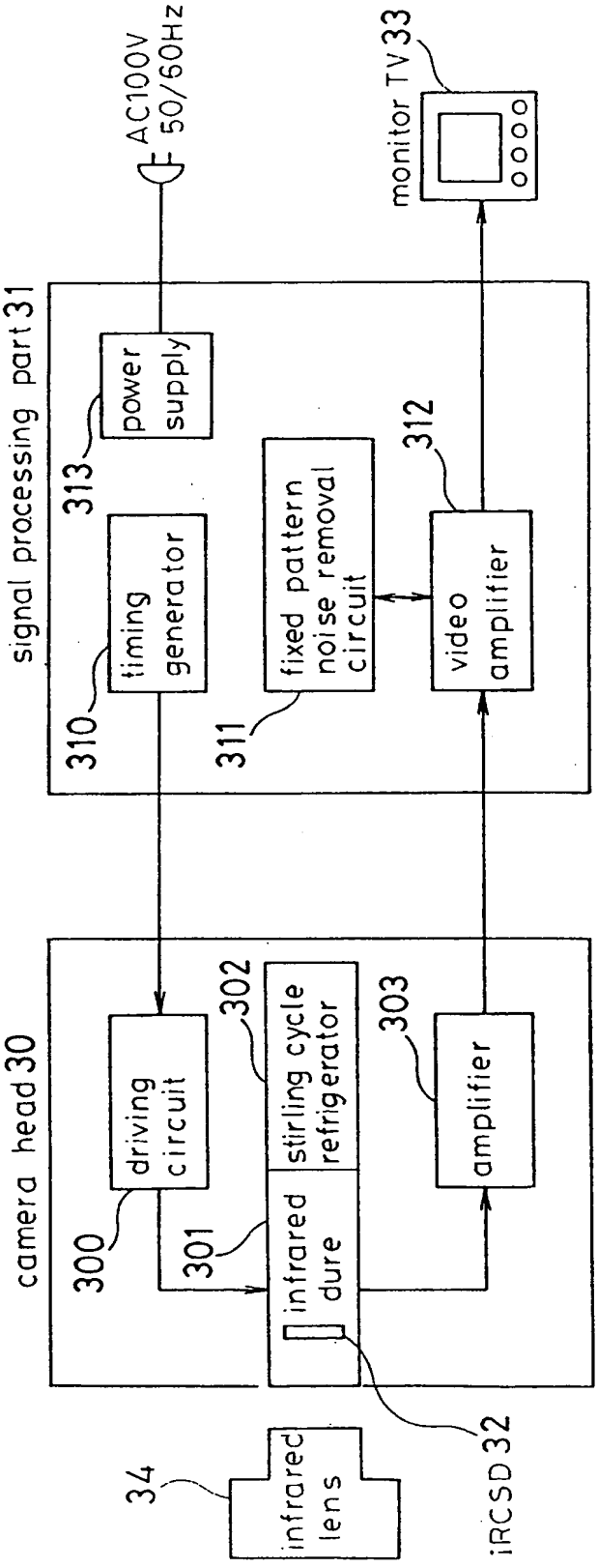


FIG. 13 (PRIOR ART)

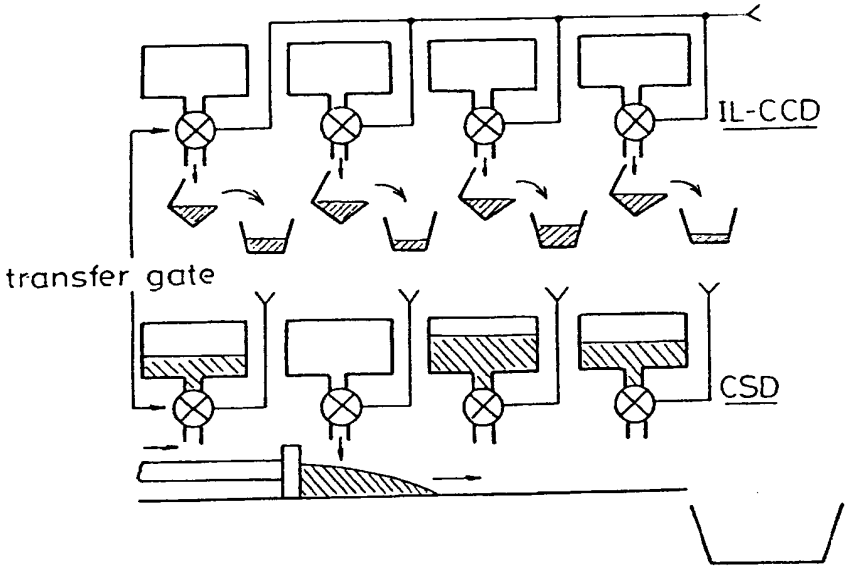


FIG. 14 (PRIOR ART)

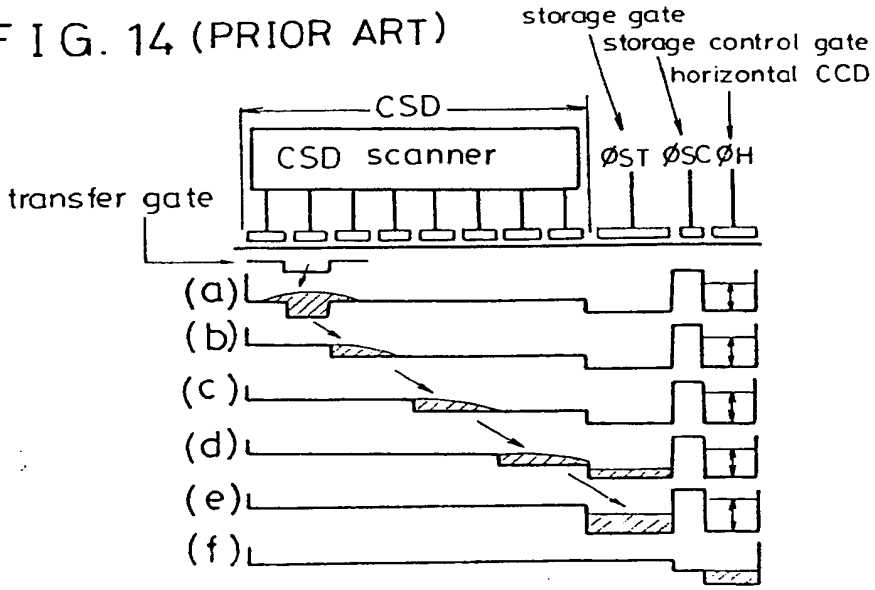
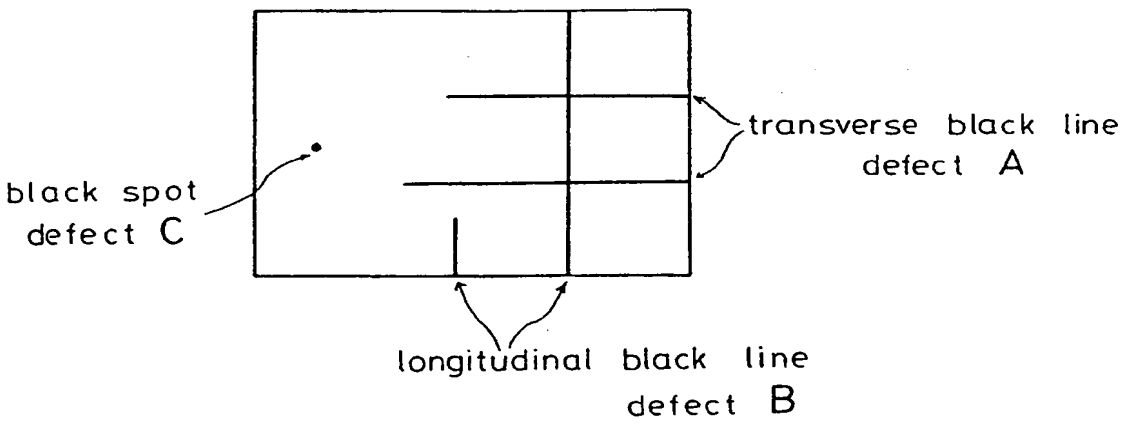


FIG. 15 (PRIOR ART)



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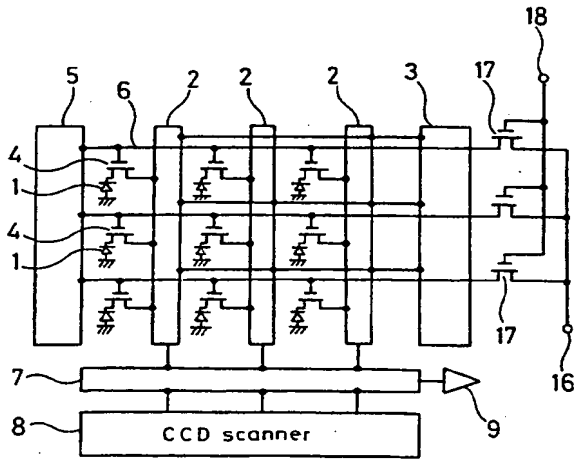
(54) **A solid state imaging element.**

(57) A solid state imaging element includes a plurality of photo detectors arranged in a two-dimensional array on a semiconductor substrate, two charge transfer circuits transferring signal charges in a vertical direction and a horizontal direction, respectively, a plurality of transfer gates controlling charge transfer from the photodetectors to one of the charge transfer circuits, a scanner controlling the switching of the transfer gates, a plurality of bus lines connecting the transfer gates with the scanner, and a bus line breakage checking means. This bus line breakage checking means includes a plurality of transistors connected with each of the bus lines in series, a test pad connected with the bus lines via the transistors and a voltage applying pad controlling the switching of the transistors. Therefore, the breakage of a bus line can be detected by a wafer test without actually operating the element, whereby time and cost required for the wafer test process and the assembly process can be reduced.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 202 905 (FUJITSU LIMITED) * page 3, line 16 - line 21; claim 1; figure 2 *	1-3	H04N17/00 H04N5/33
A	US-A-4 940 934 (KAWAGUCHI ET AL.) * column 1, line 38 - line 56; figure 1 *	1-3	
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 70 (E-485)(2517) 3 March 1987 & JP-A-61 226 955 (MITSUBISHI ELECTRIC CORP) 8 October 1986 * abstract *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04N
G01R
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 JULY 1992	MONTANARI M.

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